UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/604,165	06/28/2003	Jason P. Gill	BUR920020117US1	1164

30449 7590 07/22/2005

SCHMEISER, OLSEN + WATTS
3 LEAR JET LANE
SUITE 201
LATHAM, NY 12110

EXAMINER	
PATEL, ISHWARBHAI B	
ART UNIT	PAPER NUMBER
2841	

DATE MAILED: 07/22/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

H·A

Office Action Summary	Application No.	Applicant(s)	
	10/604,165	GILL ET AL.	
	Examiner	Art Unit	
	S Renous / Ishwar Patel	~~2748~~ 2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-30 is/are pending in the application.

4a) Of the above claim(s) 1-18 is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 19-30 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 6/28/03 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 7/21/03.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

Claims 2,3,7,8,9 are objected to because of the following informalities: the indicated claim numbers are missing. Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 19-21 are rejected under 35 U.S.C. 102(b) as being anticipated by US Patent 5,986,218 (hereafter Muto).

With regard to claim 19, Muto discloses a multilayered substrate (see FIG. 10(B)) stacked (1, 3) in the Y direction with the length of said layers being oriented in the X direction, wherein the first and second electrically conductive wires (2, 12) are within the first layer with both said wires oriented in the X direction, wherein the first and second wires are electrically and thermally coupled by a structure (13) located outside said first layer and do not physically touch, wherein a width distribution of the second wire (12) is oriented in the Z direction and is chosen so as to limit the temperature gradient to be zero or negative for all possible lengths of the multilayered substrate, wherein the

second wire's width distribution is modified in order to substantially mitigate the adverse effects of electromigration in the first wire.

With regard to claim 20, the first wire of said electrically conductive wires is coupled to a current source. In order for the wires to be conductive, there must be some source supplying current to flow through the wires.

With regard to claim 21, the electronic structure disclosed above in claims 19 and 20 includes the first wire of said electrically conductive wires which produces a mean time to failure that is minimal with respect to variations in the width of the second wire because if it were not minimal, the device would not be functional, and we assume operability of the prior art device.

Claims 19-30 are rejected under 35 U.S.C. 102(b) as being anticipated by US Patent 6,040,524 (hereafter Kobayashi).

With regard to claim 19, Kobayashi discloses a multilayered substrate (see figures 4, 5, and 6, see col. 7, lines 26-30) including layers (L_1, L_2, L_3, L_4,) stacked in the Y direction with the length of said layers being oriented in the X direction, wherein the first and second electrically conductive wires (114) are within the first layer (L_1, see col. 12, lines 58-59) with both said wires oriented in the X direction, wherein the first and second wires are electrically and thermally coupled by a structure (113, see col. 7, lines 15-19) located outside said first layer and do not physically touch, wherein a width distribution of the second wire is oriented in the Z direction and is chosen so as to limit the temperature gradient to be zero or negative for all possible lengths of the

multilayered substrate, wherein the second wire's width distribution is modified in order to substantially mitigate the adverse effects of electromigration in the first wire.

With regard to claim 20, the first wire of said electrically conductive wires is coupled to a current source (see col.12, line 60). In order for the wires to be conductive, there must be some source supplying current to flow through the wires.

With regard to claim 21, the electronic structure disclosed above in claims 19 and 20 includes the first wire of said electrically conductive wires which produces a mean time to failure that is minimal with respect to variations in the width of the second wire because if it were not minimal, the device would not be functional, and we assume operability of the prior art device.

With regard to claim 22 (see figure 6), the electronic structure disclosed above in claims 19, 20, and 21 includes a first electrically and thermally conductive via (128, see col. 13, lines 6-22) that is connected to the first wire (114) and oriented in the Y direction, wherein a second electrically and thermally conductive via (128) is connected to the second wire (114) and oriented in the Y direction; and a third electrically conductive wire (127) is contained in a third layer (L_3) of said layers, wherein the third wire's length is orientated in the X direction, wherein the second layer (L_2) is located above or below the first layer, and the third wire (127) is electrically and thermally connected to the first and second vias (128).

With regard to claim 23 (see figure 6), the electronic structure disclosed in claim 22 contains the second layer (L_2), which is disposed between the first layer (L_1) and a

device layer (L_3) of the said multilayered substrate, and wherein the second wire (114) acts as a heat sink to the first wire (114).

With regard to claim 24 and the electronic structure disclosed in claim 23, the electrical resistivity of the first wire is less than that of the second wire. It is assumed that the difference in resistivity of the two wires is a result of the variations of the width and/or cross-sectional area of one of the said conductive wires.

Claims 25 and 26 are rejected because any of Kobayashi's layers' not considered as the device layer and stacked in the substrate can be designated as the first or second layer; and the two conductive wires contained in the first layer can be designated as the first or second wire.

With regard to claim 27, the electronic structure of claim 19 contains a substrate (see figure 6) that consist of a thermally conductive layer having a thermally conductive member (L_4) and a device layer (L_2), wherein the thermally conductive member and the device layer are thermally coupled by a dielectric layer (123) disposed between the first wire (126) and the conductive member and by at least one thermally conductive via (128) disposed between the thermally conductive member (L_4) and the device layer (L_2, see col. 8, lines 1-8), wherein the dielectric layer has a sufficiently small thickness in the Y direction that permits conductive heat transfer through the thickness of the dielectric layer, and wherein the thermally conductive member does not carry an electric current . Since the operability of the prior art device is assumed, the dielectric layer is thermally conductive and therefore has a thickness that is sufficiently small.

With regard to claim 28 (see figure 6) and considering the electronic structure of claim 27, wherein the thermally conductive layer (L_2) is disposed between the first layer (L_1) and the device layer (L_4).

With regard to claim 29 (see figure 10) and considering the electronic structure of claim 27, wherein the first layer (L_5') is disposed between the thermally conductive layer (L_2') and the device layer (L_4').

With regard to claim 30 (see figure 10), the electronic structure of claim 27 includes at least one thermally conductive via (150′) that is in mechanical contact with a portion of the device layer (L_4') that does not include an active electronic device. The conductive via is connected to the device layer at a section that contains no other connections.

STEVE REMUS
FOR
LEBTHAR PATEL

KAMAND CUNEO
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

KAMAND CUNEO
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800